REMARKS

This preliminary amendment accompanies a Request for Continued Examination (RCE) and is responsive to the final Office action, mailed November 26, 2007.

As an initial matter, Applicant thanks the Examiner for allowing claims 1, 3-8 and 12-17 in the final Office action, mailed November 26, 2007.

Claims 1 and 3-18 are pending. Claims 9, 10 and 18 are currently amended. Support for the claim amendments can be found in FIG. 5. No new matter has been added.

Applicant asks that the claims be examined in view of the amendment to the claims.

Claim Rejections – 35 U.S.C. §102(a)

Claims 9 and 10 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's admitted prior art (AAPA). Applicant respectfully requests reconsideration.

Claim 9 recites a semiconductor integrated circuit device that includes an output buffer circuit with a logic gate and a driver transistor. Claim 9 has been amended to clarify that the output buffer circuit also includes a transistor switch with a plurality of transistors having different on-state resistances connected in parallel between an output of the logic gate and a control electrode of the driver transistor. An example of these features is shown in FIG. 5, in which a transistor switch is provided between an output of a nor-type logic gate NO and a gate of N-channel MOS transistor Tx. The transistor switch includes P-channel MOS transistors T7a and T7b, which have different on-state resistances (*see, e.g.*, page 15, lines 12 to 14) and which are connected in parallel.

In some implementations, the claimed subject matter results in a simplified output buffer circuit that can operate effectively regardless of whether operating frequency is low or high. Such functionality may be understood with reference to the exemplary circuit of FIG. 5, in which the on-state resistance of transistor T7a is higher than the on-state resistance of transistor T7b. *See* page 15, lines 12 to 14.

In the circuit of FIG. 5, if the operating frequency is low, then the selection control signal SELECTION turns on transistor T7a (but not T7b). This results in a higher combined resistance of the circuit to the gate of driver transistor Tx than if the transistor T7b (and not T7a) were turned on. With this higher combined resistance, changes in the gate voltage at driver transistor Tx are gradual. If, on the other hand, the operating frequency is high, then the selection control signal SELECTION turns on transistor T7b (but not T7a). This results in a lower combined resistance of the circuit to the gate of driver transistor Tx than if transistor T7a (but not T7b) were turned on. With this lower combined resistance, changes in the gate voltage at driver transistor Tx are sharp. AAPA does not disclose or render obvious the claimed subject matter.

AAPA discloses (*see, e.g.*, FIGS. 11 and 12) an output buffer circuit that includes a pair of nor-type logic gates NO1, NO2 and a MOS driver transistor Tx with a gate that receives an output from the nor-type logic gates NO1 and NO2. The circuit also includes transistor switches S1, S2, each of which is connected to a respective one of the nor-type logic gates NO1, NO2 and each of which also is connected to the gate of MOS driver transistor Tx. Each transistor switch S1, S2 has an N-channel MOS transistor Tn and a P-channel MOS transistor Tp connected in parallel. *See* FIG. 12. The nor-type logic gate NO1 has MOS transistors T1 and T4 (*see* FIG. 10) with low on-state resistances. *See* page 3, line 22 to page 4, line 1. The nor-type logic gate NO2 has MOS transistors T1 and T4 (*see* FIG. 10) with low on-state resistances. *Id.*

None of the transistors disclosed in the AAPA corresponds to the "plurality of transistors" recited in claim 9. More particularly, no set of transistors disclosed in AAPA is connected in parallel, is between an output of a logic gate and a control electrode of a driver transistor and has different on-state resistances.

N-channel MOS transistor Tn and a P-channel MOS transistor Tp in AAPA do not correspond to the "plurality of transistors" recited in claim 9. Although the N-channel MOS transistor Tn and a P-channel MOS transistor Tp in FIG. 12 are connected in parallel, AAPA is silent with respect to the relative on-state resistances of the N-channel MOS transistor Tn and P-channel MOS transistor Tp. Clearly, AAPA does not disclose that the N-channel MOS

transistor Tn and P-channel MOS transistor Tp have different on-state resistances, as recited in claim 9.

Transistor switch S1 and transistor switch S2 in AAPA also do not correspond to the "plurality of transistors" recited in claim 9. First, transistor switch S1 and transistor switch S2 are not connected in parallel, as recited in claim 9. Moreover, AAPA is silent with respect to the relative on-state resistances of transistor switch S1 and transistor switch S2. Clearly, AAPA does not disclose that transistor switch S1 and transistor switch S2 have different resistances, as recited in claim 9.

Transistors T1 and T4 in the nor-type logic gates NO1 and NO2 in AAPA also do not correspond to the "plurality of transistors" recited in claim 9. Although transistors T1 and T4 in nor-type logic gate NO1 have a different on-state resistance than transistors T1 and T4 in nor-type logic gate NO2, neither of those transistor sets is connected between an output of a logic gate and a control electrode of a driver transistor, as recited in claim 9. Instead, as FIG. 10 makes clear, those transistors T1 and T4 are inside the nor-type logic gate NO1 and NO2. Nor are the transistors T1 and T4 in logic gate NO1 "connected in parallel" with the transistors T1 and T4 in logic gate NO2, as recited in claim 9.

The series connection of logic gate NO1 and transistor switch S1 and the series connection of logic gate NO1 and transistor switch S2 also do not correspond to the "plurality of transistors" recited in claim 9. Most notably, those series connections are not connected to "the output of a logic gate," as recited in claim 9.

In some implementations, the claimed subject matter advantageously simplifies the circuitry (*e.g.,* by reducing the number of logic gates and transistor switches) and operational complexity of an output buffer circuit adaptable for use with different operational frequencies, particularly as compared to the AAPA circuitry.

Claim 9 should be allowable for at least the foregoing reasons.

Claim 10 depends from claim 9 and, therefore, should be allowable for at least the same reasons as claim 9.

Claim 18 also was rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's admitted prior art (AAPA).

Claim 18 has been amended to recite features similar to those discussed above with reference to claim 9. More particularly, claim 18 recites a semiconductor integrated circuit device that includes an output buffer circuit with a logic gate and a driver transistor. The output buffer circuit also includes a transistor switch with a plurality of transistors having different on-state resistances connected in parallel between an output of the logic gate and a control electrode of the driver transistor. For at least the reasons discussed above with reference to claim 9, AAPA does not disclose or render obvious the claimed subject matter.

Claim 18 should be allowable for at least the foregoing reasons.

Claim Rejections – 35 U.S.C. §103(a)

Claim 11 was rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art (AAPA).

Claim 11 depends from claim 9, which recites a semiconductor integrated circuit device that includes an output buffer circuit with a logic gate and a driver transistor. The output buffer circuit also includes a transistor switch with a plurality of transistors having different on-state resistances connected in parallel between an output of the logic gate and a control electrode of the driver transistor. As discussed above with reference to claim 9, AAPA does not disclose or render obvious the claimed subject matter.

Claim 11 should be allowable for at least the foregoing reasons.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or

other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a Petition for Extension of Time. The petition fee in the amount of $1,050.00 and the Request for Examination fee in the amount of $810.00 are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account Authorization. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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